

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Washington, D.C. 20231

Michael Gschwind et. al.

February 11, 2003

Serial No.:

10/085,606

Group No.: 2102

Filed:

02/26/2002

Commissioner of Patents and Trademarks

Examiner:

For: Method and Apparatus for Prioritized Instruction Issue Queue

RECEIVED

FEB 2 4 2003

Technology Center 2100

INFORMATION DISCLOSURE STATEMENT

The attached form 1449 (Modified) gives references pertaining to the above application.

Respectfully,

George Sai-Halasz Agent # 45430

Customer No.: 24,299

145 Fernwood Drive
E. Greenwich, RI 02818.
401-885-8032 (Fax 401-885-1046)
E-MAIL - patents@computer.org

24299

PATENT TRADEMARK OFFICE



Sheet 1 of 1

Form PTO 1449 (modified)							Docket No yor920020001US1		Serial No <u>10/085,606</u>						
LIST O	F PRIO	R ART CITE	D BY A	CANT	Applicant Michael Gschwind et. al.										
							Filing Date <u>02/26/200</u>	02	Group 2102						
					U.S. PATE	ENT	DOCUMENTS								
Examiner Initial		Document Number			Date		Name Cl		Class Subcla		s Filing Date				
-	AA	5,864,341		01/26/1999		Н	icks	395	39	0	12/06/1996		5		
	AB														
	•	•		FO	REIGN PA	TEI	NT DOCUMENTS	•	•		-0.0				
Examiner Initial		Document Number	Date		Name				Class Sub		RE	ling pare		/Ε[
											FE	B 2	4 ;	2003	
										 	echino.	OCV	Car	nter 21	
		ОТН	ER PRI	OR A	ART (Includ	ling A	Author, Title, Date, Pertinent Pa	iges, Et	c.)		7011110	97	001		
	C. Zilles and G. Sohi "Understanding the Backward Slices of Performance Degrading Instructions", Proc. of the International Symposium on Computer Architecture, 2000. pp: 172-181														
		K. Ebc	K. Ebcioglu, et al "Optimizations and Oracle Parallelism with Dynamic Translation", Proc. of the 32nd International Symposium on Microarchitecture, 1999. pp.: 284-295												
			S. Abraham, et al, "Predictability of Load/Store Instruction Latencies", Proc. of the 26th International Symposium on Microarchitecture, 1993. pp.:139-152												
			M. Annavaram, et al "Data Prefetching by Dependence Graph Precomputation", Proc. of the International Symposium on Computer Architecture, 2001. pp.: 52-61												
			S. Srinivasan et al, "Locality vs. Criticality", Proc. of the International Symposium on Computer Architecture, 2001,. pp.: 132-143												
Examine	er	1 1			Date Considered										
							s in conformance with MPEP 6 ommunication to applicant	09; Dr	aw line	throug	gh citatio	n if not	in		